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Abhaya Asthana received his Bachelor's degree in electrical engineering from the Indian Institute of Technology (IIT), Kanpur in 1970, and his doctorate degree from Tulane University in 1974. He led the design of VLSI systems at INTEL from 1982-1985 and was on the faculty of IIT Kanpur in 1984. He previously directed R&D in the areas of computer and communications systems and solutions, multimedia, wireless systems, converged network systems, computer architecture, operating systems, optical networks and VLSI design. He is currently a Bell Labs Fellow. He currently directs R&D within the Software and Systems Reliability Group at Bell Labs with main focus areas on the reliability of software systems with the target of achieving autonomy using techniques from analytics, modeling and machine learning.